IN THE TITLE:

The title has been amended herein. Pursuant to 37 C.F.R. §§ 1.121 and 1.125 (as amended to date), please amend the title as follows:

METHOD FOR MAKING THROUGH-HOLE CONDUCTORS FOR SEMICONDUCTOR SUBSTRATES ~~AND METHOD AND SYSTEM FOR MAKING SAME~~

IN THE SPECIFICATION:

Please amend paragraph **[0002]** as follows:

[0002] State of the Art: Integrated circuit devices are typically manufactured as individual circuits which are repeatedly formed in a pattern across the surface of a semiconductor substrate. Because of processing variations and contaminations across the surface of a semiconductor substrate, various ones of the individual integrated circuits will necessarily not function or perform as designed. Rather than identifying the defective ones of the integrated circuits at a much later stage during or after the packaging of individual integrated circuit devices, it is desirable to identify and reject defective devices at as early of a stage as possible and prior to further costly and ~~time-consuming~~ time-consuming processing and testing.

Please amend paragraph **[0008]** as follows:

[0008] In yet another embodiment of the present invention, a method of making a contactor card includes forming a hole, with an inner surface, completely through a semiconductor substrate from a first side to a second side of the semiconductor substrate and forcing a plating solution through the hole from a first plating bath to a second plating bath to deposit conductive material on the inner surface to form ~~a plated through~~ plated through-hole conductor extending from the first side to the second side.

Please amend paragraph **[0022]** as follows:

[0022] The hole 10 may further include multiple profiles which result from cleaning or other post-machining processes following the drilling or laser ablation process. For example, FIG. 1 illustrates hole 10 as being comprised of a general hole ~~profile~~ 20 and beveled end profiles 22 and 24 which may result as artifacts from a cleaning process, an example of which is a cleaning process which uses tetramethylammoniahydroxide (TMAH) for preferentially etching the crystalline structure and may cause the beveled contours illustrated as profiles 22 and 24. The formation of hole 10, regardless of any additional profiles, further results in a formation of an inner surface 26 within hole 10 whereupon electrically conductive plating material may be deposited for the formation of the pending through-hole conductor.

Please amend paragraph **[0023]** as follows:

[0023] Furthermore, substrate 12, in one embodiment, is comprised of a semiconductive material which, if directly coupled to a contact pad of a wafer-under-test having integrated circuits thereon, may present undesirable loading or shorting to the electronic circuitry under test. Therefore, the formation of a conductor between the first and second sides is isolated from substrate 12 through the formation of an insulator material layer 28. In one embodiment of the present invention, insulator material layer 28 is comprised of a TEOS or LSO material deposited within hole 20 to provide a barrier isolation between substrate 12 and a forthcoming formation of a through-hole conductor. Other insulator materials may include silicon dioxide formed from the substrate material and a ~~Parylene™~~ PARYLENE™ coating, available from Specialty Chemical Coatings. The insulator material layer 28 further provides crosstalk isolation between any other adjacent conductors.

Please amend paragraph **[0025]** as follows:

[0025] The seed layer 27 is coated with a conductive layer of metal forming conductive plating 36 as illustrated in FIG. 2, according to an electroless deposition process. The conductive plating 36 is deposited on the seed layer 27 of the substrate 12 and may comprise any type of metal including, but not limited to, nickel, cobalt, copper, silver, aluminum, titanium, iridium, gold, tungsten, tantalum, molybdenum, platinum, palladium, nickel-phosphorus (NiP), ~~palladium-phosphorus~~ palladium-phosphorus (Pd-P), cobalt-phosphorus (Co-P), a Co-W-P alloy, other alloys of the foregoing metals and mixtures thereof. The type and thickness of the conductive plating 36 will vary depending on the desired conductivity and use of the interconnect and may be determined, at least in part, by the resistance (R) of the metal or conductive layer expressed by the equation $R = \rho L/A$ as known in the art.

Please amend paragraph **[0026]** as follows:

[0026] By coating the seed layer 27 with the conductive plating 36 of a suitable metal, an annular conductive path is created through the hole 20 (FIG. 2). The electroless plating

process forms a substantially conformal coating in the hole 20 that is substantially free of any voids or keyholes. The conductive layer formed from the electroless plating process will typically have a uniform thickness, a low porosity, will provide corrosion protection and will be relatively hard. The electroless plating process is accomplished by placing the substrate 12 into a bath containing an aqueous solution of the metal to be deposited in ionic form. The aqueous solution also includes a chemical reducing agent such that the metal may be deposited without the use of electrical energy. The driving force for the reduction of the metal ions and subsequent deposition in the electroless plating process is driven by the chemical reducing agent. The reduction reaction is essentially constant at all points on the seed layer 27 so long as the aqueous solution is sufficiently agitated by pressurized flow to ensure that a uniform concentration of metal ions and reducing agents ~~are distributed~~ is distributed in the aqueous solution.

Please amend paragraph **[0027]** as follows:

[0027] FIG. 2 illustrates a through-hole conductor formed in accordance with an embodiment of the present invention. A through-hole conductor 30 is formed between first and second sides 14 and 16 through substrate 12 by forcing the plating solution (not shown) from a high-pressure side of substrate 12 in a flow direction 32 to a low-pressure side in a flow direction 34 thereof. Due to the passage of plating solution in this directed flow process, conductive plating 36 forms on inner surface 26 in a generally uniform manner. Due to the pressurized flow of the plating solution, substantially uniform plating results when fresh plating solution having a generally uniform concentration passes through the physical hole 10 within substrate 12 followed by the periodic cycling of power in the electroplating process. The cycling of the power is timed and sequenced to allow fresh fluid or uniform concentrated fluid to pass into the ~~hole~~ hole 10 prior to the reactivation of the electroplating power. Electroplating may be preceded by an electroless, or immersion plating process to deposit gold, nickel or other suitable metal layer on the sidewalls of hole 20 to facilitate the electroplating. It is appreciated that at some point in time in such a continuous process, the formation of conductive plating 36 may build up and result in a physical barrier between the high-pressure side and the low-pressure side thereby restricting the flow of plating solution therebetween.

Please amend paragraph **[0030]** as follows:

[0030] The plating fixture 42 further includes a coupling means 46 to facilitate the coupling of semiconductor substrate 44 with plating fixture 42. While a mechanical coupling mechanism comprising a clamp is illustrated, other arrangements may include a vacuum coupling mechanism, an adhesive-based mechanism or other similar attachment for attaching a cooperative barrier mechanism to the semiconductor substrate 44. Furthermore, utilization of a plating fixture 42 is illustrated as but one technique for forming a boundary between high- and low-pressure sides within a plating system. Also contemplated within the scope of the present invention is the formation of a barrier between high- and low-pressure sides by way of the semiconductor substrate itself without the use of a fixturing mechanism. Furthermore, coupling ~~mechanism~~ means 46 may provide electrical coupling to a substrate 12 for facilitating an electroplating process. Also contemplated are flow bypass mechanisms 48 which may facilitate the circulation of higher concentration plating solutions to staged substrates in sequence in a multisubstrate arrangement without requiring the solution to first pass through an "upstream" semiconductor wafer or substrate 44.

Please amend paragraph **[0033]** as follows:

[0033] While plating solutions, being liquid in nature, are essentially incompressible, flow direction 78 is maintained by pressurizing the plating solution in bath 80. Furthermore, as the through-hole conductors 30 (FIG. 2) on loaded fixtures 88-92 become ~~plated through,~~ plated through, flow of the plating solution to the next successive bath becomes more restricted. Therefore, it may be desirable in a multiple wafer plating system 70 to include flow bypass mechanisms 48 (FIG. 3) on at least "upstream" loaded fixtures in order to facilitate flow of the plating solution to subsequent baths.

Please amend paragraph **[0038]** as follows:

[0038] FIG. 9 illustrates incorporation of a through-hole conductor into a connector card and further into an interconnection system 160, in accordance with embodiments of the

present invention. A connector card 166 functions as an intermediary coupling means for conducting one or more electrical contacts (e.g., contact pads) between two separate conductive interfaces, an example of which is shown as a printed circuit board (hereinafter "PCB") 162 and a wafer or other semiconductor substrate 176 bearing a plurality of integrated circuits. FIG. 9 illustrates, by way of example and not limitation, a pad 164 on PCB 162 coupling with a conductive cap 168 on through-hole conductor 170. Similarly, a conductive cap 178 on a wafer or substrate 176 couples to a through-hole conductor 174 which, in turn, couples to the through-hole conductor 170 via a conductive trace 172. Interconnection system 160 may be a portion of a testing system with wafer or substrate 176 being a wafer-under-test and PCB 162 being a portion of a testing system ~~such a~~ such as a probe card from a tester.